**CS 520 - Fall 2013   
Homework 3**

**Due: Friday, November 22 at the beginning of class**

1. [30%] Consider the following stream of memory word addresses directed at the cache. Assume that the memory is word addressable, and the total cache capacity is 64 words. Further assume that the cache is 2-way set-associative, the cache line size is 8 words and the LRU replacement policy is used.

5, 7, 1, 12, 34, 39, 65, 3, 107

For each of these accesses, indicate whether it is a cache hit or a cache miss, show how you computed the cache index, and depict the contents of the cache after every access. You do not have to show the tag bits, only show the addresses of the cached data.

1. [30%] Consider a system with physically-addressed caches, and assume that 40-bit virtual addresses and 32-bit physical addresses are used, and the memory is byte-addressable. Further assume that the cache is 4-way set-associative, the cache line size is 64 Bytes and the total size of the cache is 64 KBytes. Answer the following questions, providing adequate explanations in all cases:
2. What should be the minimum page size in this system to allow for the overlap of the TLB access and the cache access?
3. Repeat part (a) assuming that the cache associativity is increased to 8. Assume that the total cache size and the cache line size remain the same.
4. Assuming that the memory page size in this system is as calculated in your answer to Part (b), compute the total size of the page table in bytes. Assume that a simple linear page table is used and only the page translation information is stored in each entry, with no additional bits.
5. Repeat part (b) assuming that the OS can guarantee that the two least significant bits of the page number would not change during the address translation.
6. Assume that the OS needs to establish a mapping for the virtual page number 52356 (expressed in decimal). List some possible frame numbers in the physical memory where this page can be mapped to support the OS guarantee described in part (d).
7. [40%] Consider the use of multi-level hot-cold bits in implementing a replacement algorithm for a set-associative cache with 2p ways and S sets. This is an approximation of the LRU policy that marks the most recently assessed way as hot, and the other one as cold (for a 2-way set-associative cache). This mechanism can be extended to more than two ways by providing multiple levels of hot-cold bits. For example, for a 4-way cache the victim is determined as the cold way of the cold pair.
8. What is the total number of hot-cold bits for each set in this cache?
9. What is the total number of hot-cold bits in the cache?
10. Assume that p = 2 and accesses to a specific set result to the following ways in sequence and no misses occur:

Way 0, Way 3, Way 2, Way 0, Way 1, Way 1, Way 2, Way 3, Way 2, Way 0

At the end of the fifth access in this sequence (to Way 1), what are the settings of the hot-cold bit? Do they point to the same victim that would have been selected by a true-LRU algorithm?

1. Repeat Part (c), assuming that the all accesses shown in the sequence given in Part (c) have been completed with the last access being made to Way 0.